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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,770	01/26/2004	David Presley Wallace	72214	9761

27975 7590 09/15/2008

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER
LOUIE, OSCAR A

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
09/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

Office Action Summary	Application No.	Applicant(s)	
	10/764,770	WALLACE ET AL.	
	Examiner	Art Unit	
	OSCAR A. LOUIE	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This first non-final action is in response to the original filing of 06/23/2008. Claims 2-5 & 7-9 are pending and have been considered as follows.

Examiner Note

In light of the applicants' amendments, the examiner hereby withdraws his previous Claim Objections with respect to Claims 2, 5, 7 & 8.

Claim Objections

1. Claims 2, 5, & 7 are objected to because of the following informalities:

   - Claim 2 line 5 recites the term "operatively" which should be omitted;
   - Claim 5 line 5 recites the term "operatively" which should be omitted;
   - Claim 7 line 5 recites the term "operatively" which should be omitted;

   Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 7 line 25 recites "the processor" however, it appears that the applicant has defined two different processors on lines 4 & 12 with "a processor"; thus, it is unclear as to whether "the processor" is the same processor;

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5 & 7-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Sutherland (US-6292898-B1).

Claim 2:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus (and a processor operatively connected to the security key memory), a

method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- "(a) monitoring the integrity of said housing" (i.e. "A detector 303 is adapted, as described in more detail below, to detect an intrusion into the secure environment") [column 5 lines 52-53];
- "(b) in response to step (a) detecting said compromise in the integrity of said housing (using the processor)" (i.e. "detect an intrusion into the secure environment") [column 5 lines 52-53];
- "changing the contents of said security key memory (by using the processor to scramble the contents of the security key memory) so as to effectively remove said security key from said security key memory" (i.e. "electrical current is either supplied from a reference voltage generator 305 to the volatile data storage device 301 or sourced to the reference voltage generator 305 from the volatile data storage device 301 to effect erasure of data stored in the volatile data storage device") [column 5 lines 59-63];
- "wherein step (a) comprises storing, in a single-bit storage device, a single bit representative of a prescribed power supply state of said security key memory" (i.e. "volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells") [column 6 lines 9-16];

- "changing the bit state, of said single-bit storage device in response to said compromise in the integrity of said housing for said memory such that (the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory)" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22];

but, Sutherland does not explicitly disclose in the same embodiment,

- "a processor operatively connected to the security key memory" and "by using the processor to scramble the contents of the security key memory" and "the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," although Sutherland does suggest at least one prior art system that utilizes a processor, as recited below as admitted prior art;

however, Sutherland does disclose,

- [Fig 2 illustrates a prior art system that utilizes a processor];
- "…When an intrusion is detected, a processor 204 causes data stored within the volatile data storage device 201 to be erased or changed so that the originally stored data cannot be ascertained. The processor 204 may also make use of other devices (not shown), as appropriate or necessary, to effect destruction of the data" [column 3 lines 8-14];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a processor operatively connected to the security key memory" and "by using the processor to scramble the contents of the security key memory" and "the

processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," in the invention as disclosed by Sutherland since Sutherland had admitted that the inclusion of a processor is present in prior art systems that his invention improves upon, where the processor is used for the purposes of handling all of the method steps recited in the invention as disclosed by Sutherland.

Claim 3:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus and a processor operatively connected to the security key memory, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 2 above, further comprising,

- "wherein step (b) comprises in response to step (a) detecting a change in the bit state of said single-bit storage device" (i.e. "When the voltages at the designated input nodes become equal, the data retention voltages in the volatile data storage device 301 become equal as well") [column 6 lines 25-27];
- "changing the contents of said security key memory so as to effectively remove said security key from said security key memory" (i.e. "Since the data retention voltages are equal, each memory cell of the volatile data storage device 301 stores the same value and, thus, all of the data stored in the volatile data storage device 301 is effectively erased") [column 6 lines 27-31].

Claim 4:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus and a processor operatively connected to the security key memory, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 2 above, further comprising,

- "wherein step (a) comprises coupling a switch, having a closure state dependent upon the integrity of said housing, to said single-bit storage device" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22];
- "in response to said compromise in the integrity of said housing, operating said switch, so as to change the bit state of said single-bit storage device" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22].

Claim 5:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory in which is stored a security key that enables a user to operate said electronic signal processing apparatus and (a processor operatively connected to the security key memory), an arrangement configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- "a single-bit storage device which is (coupled to the processor) and coupled to store a single bit representative of a prescribed power supply state of said security key memory" (i.e. "volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells") [column 6 lines 9-16];
- "a switch, which is coupled to said single-bit storage device, and is configured to change the bit state thereof in response to said compromise in the integrity of said housing for said memory" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22];
- "wherein (said processor is configured in response to said change in the bit state of said single-bit storage device, to change the contents of said security key memory) so as to effectively remove said security key from said security key memory by scrambling the contents of the security key memory, (said processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory)" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22];

but, Sutherland does not explicitly disclose in the same embodiment,

- "a processor operatively connected to the security key memory" and "coupled to the processor" and "said processor is configured in response to said change in the bit state of said single-bit storage device, to change the contents of said security key memory" and "said processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," although Sutherland does suggest at least one prior art system that utilizes a processor, as recited below as admitted prior art;

however, Sutherland does disclose,

- [Fig 2 illustrates a prior art system that utilizes a processor];
- "…When an intrusion is detected, a processor 204 causes data stored within the volatile data storage device 201 to be erased or changed so that the originally stored data cannot be ascertained. The processor 204 may also make use of other devices (not shown), as appropriate or necessary, to effect destruction of the data" [column 3 lines 8-14];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a processor operatively connected to the security key memory" and "coupled to the processor" and "said processor is configured in response to said change in the bit state of said single-bit storage device, to change the contents of said security key memory" and "said processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," in the invention as disclosed by Sutherland since Sutherland had admitted that the inclusion of a processor is present in prior art systems that his invention improves upon, where the processor is used for the purposes of handling all of the method steps recited in the invention as disclosed by Sutherland.

Claim 7:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus and (a processor operatively connected to the security key memory), an arrangement configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- "an intrusion detection circuit that is configured to monitor the integrity of said housing" (i.e. "A detector 303 is adapted, as described in more detail below, to detect an intrusion into the secure environment") [column 5 lines 52-53];
- "(a processor) that is configured, in response to said intrusion detection circuit detecting a compromise in the integrity of said housing, to modify the contents of said security key memory and thereby effectively remove said security key from said security key memory by (scrambling the contents of the security key memory)" (i.e. "electrical current is either supplied from a reference voltage generator 305 to the volatile data storage device 301 or sourced to the reference voltage generator 305 from the volatile data storage device 301 to effect erasure of data stored in the volatile data storage device") [column 5 lines 59-63];
- "wherein said intrusion detection circuit includes a single-bit storage device that is configured to store a single bit representative of a prescribed power supply state of said security key memory" (i.e. "volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to

enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells") [column 6 lines 9-16];

- "a switch that is configured to change the bit state of said single-bit storage device in response to said compromise in the integrity of said housing for said memory, wherein (the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory)" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22];

but, Sutherland does not explicitly disclose in the same embodiment,

- "a processor operatively connected to the security key memory" and "a processor… scrambling the contents of the security key memory" and "the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," although Sutherland does suggest at least one prior art system that utilizes a processor, as recited below as admitted prior art;

however, Sutherland does disclose,

- [Fig 2 illustrates a prior art system that utilizes a processor];
- "…When an intrusion is detected, a processor 204 causes data stored within the volatile data storage device 201 to be erased or changed so that the originally stored data cannot be ascertained. The processor 204 may also make use of other devices (not shown), as appropriate or necessary, to effect destruction of the data" [column 3 lines 8-14];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a processor operatively connected to the security key memory" and "a processor… scrambling the contents of the security key memory" and "the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory," in the invention as disclosed by Sutherland since Sutherland had admitted that the inclusion of a processor is present in prior art systems that his invention improves upon, where the processor is used for the purposes of handling all of the method steps recited in the invention as disclosed by Sutherland.

Claim 8:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus and (a processor operatively connected to the security key memory), an arrangement configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 7 above, further comprising,

- "said memory contents modification circuit is configured, in response to a change in the bit state of said single-bit storage device, to change the contents of said security key memory so as to effectively remove said security key from said security key memory" (i.e. "Since the data retention voltages are equal, each memory cell of the volatile data storage device 301 stores the same value and, thus, all of the data stored in the volatile data storage device 301 is effectively erased") [column 6 lines 27-31].

Claim 9

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus and (a processor operatively connected to the security key memory), an arrangement configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 8 above, further comprising,

- "said switch has a closure state dependent upon the integrity of said housing" (i.e. "the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal") [column 6 lines 18-22].

Response to Arguments

6. Applicant's arguments filed 06/23/2008 have been fully considered but they are not persuasive.

- The applicant's remarks on pages 6-7 have been carefully considered but are non-persuasive. The examiner notes that the applicant appears to be arguing what was already present in the prior art reference as admitted prior art by the reference itself, which does not overcome the current rejection.

See section 2123:

> *Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In re Susi, 440 F.2d 442, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994) (The invention was directed to an epoxy impregnated fiber-reinforced printed circuit material. The applied prior art reference taught a printed circuit material similar to that of the claims but impregnated with polyester-imide resin instead of epoxy. The reference, however, disclosed that epoxy was known for this use, but that epoxy impregnated circuit boards have "relatively acceptable dimensional stability" and "some degree of flexibility," but are inferior to circuit boards impregnated with polyester-imide resins. The court upheld the rejection concluding that applicant's argument that the reference teaches away from using epoxy was insufficient to overcome the rejection since "Gurley asserted no discovery beyond what was known in the art." 27 F.3d at 554, 31 USPQ2d at 1132.). Furthermore, "[t]he prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).*

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/OAL/
09/09/2008

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136